Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A system for writing data, comprising:

a memory configured to store data units;

at least one memory controller configured to:

receive a first write request associated with a data unit,

store the data unit in the memory, and

transmit a first reply including a first address where the data unit is stored; and

control logic configured to:

receive the first reply, and

determine whether the first address differs from an address included in at least one other reply by at least a first value.

2. (original) The system of claim 1, wherein the control logic is further configured to:

initiate a corrective action when the first address differs from the address included in the at least one other reply by at least the first value.

3. (original) The system of claim 2, wherein the control logic is further configured to:

suspend the corrective action when a second address included in a second reply differs from an address included in at least one other reply by less than a second value.

4. (original) The system of claim 1, wherein the memory comprises a plurality of memory devices and the at least one memory controller comprises a plurality of memory controllers, the system further comprising:

a request engine configured to:

generate the first write request, and

transmit the first write request to a first one of the memory controllers; and

wherein the first memory controller is configured to determine where to store the data unit associated with the first write request.

5. (original) The system of claim 1, wherein the at least one memory controller is configured to increment its address register by a first predetermined value after a data unit is stored.

6. (original) The system of claim 5, wherein the at least one memory controller is configured to:

receive a second write request indicating that a value in its address register is outside a predetermined range,

store a second data unit associated with the second write request, and

increment its address register by a second predetermined value after the second data unit is stored.

7. (original) The system of claim 6, wherein the at least one memory controller is further configured to:

transmit a second reply including a second address where the second data unit is stored; and wherein the control logic is further configured to:

determine whether the second address differs from an address included in at least one other reply by less than a second value.

8. (original) The system of claim 6, wherein the first predetermined value is less than a second predetermined value.

9. (original) A method for processing data, comprising:

receiving a first write request associated with a data unit;

storing the data unit;

transmitting a first reply including a first address where the data unit is stored; and

determining whether the first address differs from an address included in at least one other reply by at least a first value.

10. (original) The method of claim 9, further comprising:

initiating a corrective action when the first address differs from the address included in the at least one other reply by at least the first value.

11. (original) The method of claim 10, further comprising:

suspending the corrective action when a second address included in a second reply differs from an address included in at least one other reply by less than a second value.

12. (previously presented) The method of claim 9, further comprising:

generating the first write request, the first write request including the data unit;

transmitting the first write request to a first memory controller; and

wherein the storing the data unit includes:

determining, by the first memory controller, where to store the data unit.

13. (original) The method of claim 9, further comprising:

incrementing an address register by a first predetermined value after the data unit is stored.

14. (original) The method of claim 13, further comprising:

generating a second write request indicating that a value in the address register is outside a predetermined range;

storing a second data unit associated with the second write request; and

incrementing the address register by a second predetermined value after the second data unit is stored.

15. (original) The method of claim 14, further comprising:

transmitting a second reply including a second address where the second data unit is stored; and

determining whether the second address differs from an address included in at least one other reply by less than a second value.

16. (original) The method of claim 14, wherein the first predetermined value is less than a second predetermined value.

17. (currently amended) A network device, comprising:

a plurality of memory banks configured to store data units;

a plurality of request engines configured to generate write requests, the write requests each including at least one data unit; ~~and~~

a plurality of memory controllers, each memory controller being configured to:

receive a write request,

determine where to store the data unit included in the write request using an address register associated with the memory controller, ~~and~~

store the data unit at a location identified by the address register, and

transmit a message identifying the location where the data unit is stored; and

logic configured to:

receive the message, and

determine whether the location where the data unit is stored differs from a location included in at least one other message by at least a first value.

18. (previously presented) The network device of claim 17, wherein a number of the data units comprise a data packet and each of the plurality of memory controllers is further configured to:

increment the address register after storing the data unit.

19. (previously presented) The network device of claim 17, wherein each of the memory controllers includes an address register.

20. (original) The network device of claim 19, wherein each of the memory controllers is configured to:

receive write requests from the plurality of request engines, and

store data units included in the write requests in a memory bank, the data units being stored at respective locations identified by its address register.

21. (previously presented) The network device of claim 17, wherein the write requests do not include information identifying a particular location in one of the plurality of memory banks.

22. (previously presented) The network device of claim 17, wherein the write requests include information identifying an amount by which the memory controller receiving the write request is to increment the address register.

23. (previously presented) A method for writing data in a network device, comprising:

generating write requests, each write request including at least one data unit, wherein a number of the data units comprise a data packet;

forwarding the write requests to one of a plurality of memory controllers;

determining, by a first one of the memory controllers, where to store a data unit included in a write request using an address register;

storing the data unit at a first address identified by the address register;

determining whether the first address differs from an address associated with at least one other stored data unit by a first value; and

initiating a corrective action when the first address differs from the address associated with the at least one other stored data unit by at least the first value.

24. (previously presented) The method of claim 23, wherein the write requests include information identifying an amount by which to increment the address register, the method further comprising:

incrementing the address register by a first value or a second value, based on information included in the write request.

25. (original) A system for writing data, comprising:

a plurality of memory devices configured to store data units, a number of the data units comprising a data packet;

a plurality of memory controllers corresponding to the plurality of memory devices;

a plurality of address registers associated with the plurality of memory controllers, a first one of the memory controllers being configured to:

receive a first data unit, and

store the first data unit in a first one of the memory devices, the first data unit being stored at a location identified by a first one of the address registers; and

control logic configured to:

determine a difference between a value of the first address register and a value of at least one of the other address registers, and

determine whether the difference is greater than a first threshold.

26. (original) The system of claim 25, wherein the control logic is further configured to:

generate, when the difference is greater than the first threshold, a signal indicating that the first address register is outside a predetermined range, and

transmit the signal to the first memory controller.

27. (original) The system of claim 26, wherein the first memory controller is further configured to:

receive a second data unit,

store the second data unit in the first memory device, and

increment the first address register by a value of at least two, in response to receiving the signal from control logic.

28. (original) The system of claim 27, wherein the control logic is further configured to:

continue incrementing the first address register by a value of at least two until a maximum difference between a current value of the first address register and a current value of each of the other address registers is less than a second threshold.

29. (original) A system for writing data, comprising:

a plurality of memory banks configured to store data units, a number of the data units comprising data packets, wherein at least some of the data units associated with a first data packet are stored in different memory banks;

a write request engine configured to generate write requests, each write request including a data unit;

a plurality of memory controllers corresponding to the plurality of memory banks, each of the memory controllers including an address register, a first one of the memory controllers being configured to:

receive a first write request,

store the data unit included in the first write request in a first one of the memory banks,

increment its address register, and

transmit a first reply including a write pointer, the write pointer identifying an address where the data unit is stored; and

control logic configured to:

receive the first reply,

determine a difference between the write pointer in the first reply and write

pointers included in replies from each of the other memory controllers,

identify the maximum difference, and

determine whether the maximum difference is greater than a first threshold.

30. (original) The system of claim 29, wherein the control logic is further configured to:

transmit a signal to the write request engine indicating that the maximum difference is greater than the first threshold.

31. (original) The system of claim 30, wherein the write request engine is further configured to:

generate a second write request, the second write request indicating that the address register is to be incremented by a value of at least two, in response to receiving the signal from control logic, and

transmit the second write request to the first memory controller.

32. (original) The system of claim 31, wherein the control logic is further configured to:

continue generating write requests indicating that the address register is to be incremented by a value of at least two until a determined difference between a write pointer in a reply associated with the first memory controller and a write pointer included in a reply associated with each of the other memory controllers is less than a second threshold.

33. (original) A system for writing data in a network device, comprising:

means for storing data cells in one of a plurality of memory banks, a number of the data cells comprising data packets and at least some of the data cells being associated with a first data packet being stored in different memory banks;

means for determining whether a pointer associated with any one of the memory banks is outside a predetermined range; and

means for adjusting the memory bank that is outside the predetermined range.

34-37. (canceled)